SGS-THOMSON MICROELECTRONICS

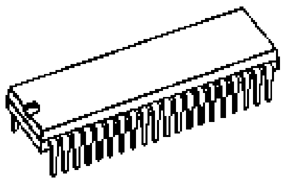
M491B

SINGLE-CHIP VOLTAGE SYNTHESIS TUNING SYSTEM WITH 1 ANALOG CONTROL

- 16-STATION MEMORY - 7-SEGMENT LED DISPLAY
- VOLTAGE SYNTHESIZER : 13 BITS
- 4-BAND PRESET CAPABILITY
- NON-VOLATILE MEMORY : 304 BITS
  - 16 WORDS OF 19 BITS FOR TUNING VOLTAGE (13 bits) - BAND (2 bits) - FINE DETUNING (4 bits)
  - 10^4 MODIFY CYCLES PER WORD
  - MIN 10 YEARS DATA RETENTION
- PCM REMOTE CONTROL RECEIVER : DECODES SIGNAL TRANSMITTED BY M708
- VOLUME D/A : 6-BIT RESOLUTION / 8kHz
- MEMORY SKIP FUNCTION
- AUTOMATIC SEARCH WITH DIGITAL AFT CONTROL
- FINE DETUNING D/A ACTING ON AFT DISCRIMINATOR (16 steps) WITH SEPARATE STORAGE FOR EACH MEMORY POSITION. ALTERNATIVELY IT CAN BE USED TO CONTROL BRIGHTNESS OR COLOUR SATURATION
- MANUAL SEARCH WITH DIGITAL AFT CONTROL
- MANUAL SEARCH WITH LINEAR AFT
- SWEEP SEARCH DISPLAY OUTPUT
- SUPPLY VOLTAGES : V_{DD} = + 5V, V_{PP} = + 25V FOR THE MEMORY
- CLOCK OSCILLATOR : 445 TO 510kHz
- INTEGRATED DIGITAL POWER ON RESET (no external initialization circuitry required)

DESCRIPTION

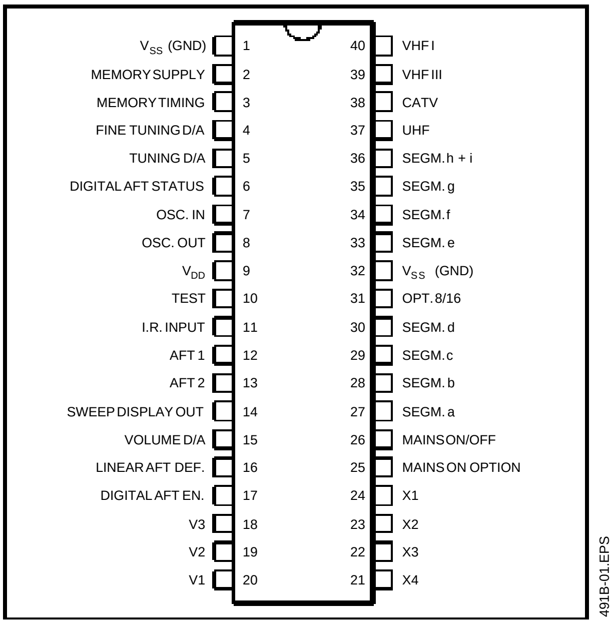
The M491B is a monolithic N-MOS LSI circuit including a Floating-gate Non-Volatile Memory for storage of up to 16 stations. Tuning of the station is performed with a 8192 step D/A converter, using the principle of voltage synthesis. It is designed for 7-segment LED displays. Direct memory selection is possible only from remote control while Up/Down memory scanning is possible on the set and also from remote control. An option input for 8 or 16 stations is available. The circuit also includes a PCM remote control receiver operating in conjunction with the transmitter M708. The highly reliable transmission code ensures error-free signal detection even in presence of high noise conditions. Search of the station is possible in automatic or manual modes. The circuit can operate with a Digital or Linear AFT control. The Digital AFT mode is necessary for automatic search and requires an external circuit (TDA4433 or equivalent, e.g. dual comparator plus TV station detector) to convert the AFC-S-curve into an Up/Down command. Fine tuning (detuning) is also possible with different modes of operation. The circuit is assembled in 40-pin dual in-line plastic package.



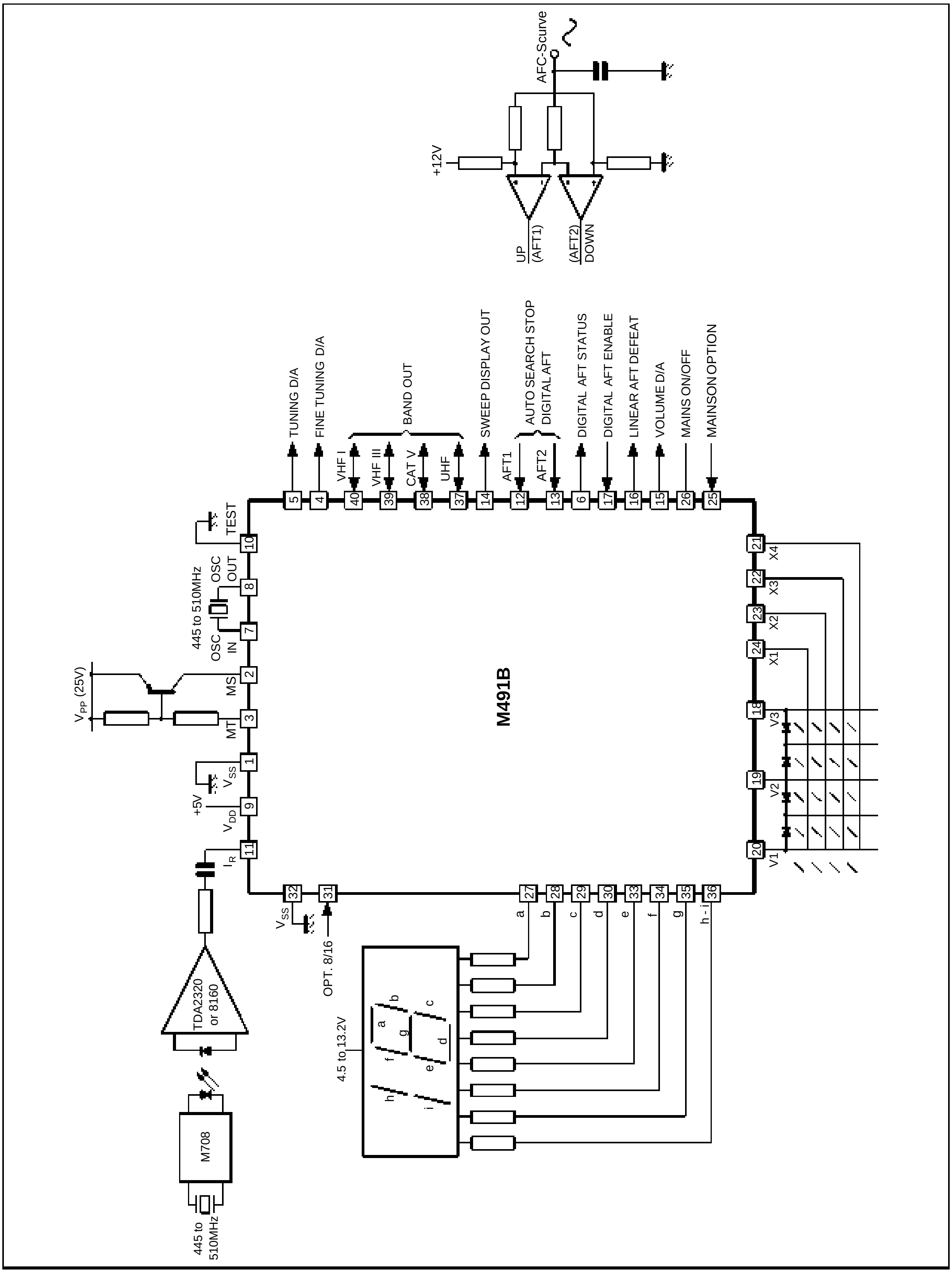
DIP40
(Plastic Package)

ORDER CODE : M491B1

PIN CONNECTIONS



FUNCTIONAL DIAGRAM



491B-02.EPS

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage	– 0.3, + 7	V
V_{PP}	Memory Supply Voltage	– 0.3, + 26	V
V_I	Input Voltage	– 0.3, + 15	V
$V_{O\ (off)}$	Off State Input Voltage (except pin 3) Pin 3	15 28	V V
I_{OL}	Output Low Current Led Driver Outputs Pins 6 – 14 Pins 4 – 5 All Other Outputs	 20 20 7.5 5	mA
t_{pd}	Max. Delay between Memory Timing and Memory Supply Pulses	5	µs
P_{tot}	Total Package Power Dissipation	1	W
T_{stg}	Storage Teperature	– 25, + 125	°C
T_{op}	Operating Temperature	0, + 70	°C

491B-01.TBL

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

(T_{amb} = 0 to + 70°C, V_{DD} = +5V unless otherwise specified)

Pin	Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
2-Memory Supply	I_{PP}	Memory Supply Current	V_{PP} = 25V Write Peak Average Erase Peak Average Read Peak Average			 42 12 9 5 8 2.5	mA
	R	Pull Down Resistor				25	kΩ
3–Write Timing Out	V_{OL}	Output Low Voltage	V_{DD} = 4.75 V, I_{OL} = 2.5 mA			8	V
	$I_{O\ (off)}$	Output Leakage Current	V_{DD} = 4.75 V, V_{OUT} = 26 V			100	µA
4–Fine Tuning D/A 5–Tuning D/A	$I_{O\ (off)}$		V_{DD} = 5.25 V, $V_{O\ (off)}$ = 13.2 V			50	µA
	V_{OL}		V_{DD} = 4.75 V, I_{OL} = 5 mA			1	V
6–Digital AFT Out	V_{OL}		V_{DD} = 4.75 V, I_{OL} = 20 mA			1.5	V
	$I_{O\ (off)}$		V_{DD} = 5.25 V, $V_{O\ (off)}$ = 13.2 V			100	µA
9–Power Supply	I_{DD}	Supply Current	V_{DD} = 5.25 V			100	mA
11–I.R. Input	V_{IPP}	Peak-to-Peak Voltage		0.5		13.2	V
12–AFT1 13–AFT2	V_{IL}	Input low Voltage	V_{DD} = 5.25 V			1.5	V
	V_{IH}	Input High Voltage	V_{DD} = 5.25 V	3.5			V
	I_{IL}	Input Low Current	V_{DD} = 5.25 V, V_{IL} = 1.5 V			–0.4	mA
	R	Pull-up Resistor			30		kΩ
14—Display Out	V_{OL}		V_{DD} = 4.75 V, I_{OL} = 20 mA			1.5	V
	$I_{O\ (off)}$		V_{DD} = 5.25 V, $V_{O\ (off)}$ = 13.2 V			100	µA
15–Volume D/A	V_{OL}		V_{DD} = 4.75 V, I_{OL} = 4 mA			1	V
	$I_{O\ (off)}$		V_{DD} = 5.25 V, $V_{O\ (off)}$ = 13.2 V			50	µA
16–Linear AFT Out	V_{OL}		V_{DD} = 4.75 V, I_{OL} = 1 mA			0.4	V
	$I_{O\ (off)}$		V_{DD} = 5.25 V, $V_{O\ (off)}$ = 13.2 V			50	µA
17–Digital AFT Enable	V_{IL}					0.8	V
	V_{IH}			2.0			V
	I_{IL}		V_{DD} = 5.25 V, V_{IL} = 0.8 V			–0.4	mA
	R	Pull-up Resistor			30		kΩ

491B-02.TBL

DC ELECTRICAL CHARACTERISTICS (continued)

Pin	Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
18–19–20 V3, V2, V1 } Keyboard In	V_{IL}					1.5	V
	V_{IH}			3.5			V
	I_{IL}		V_{DD} = 5.25 V, V_{IL} = 0.8 V			–0.4	mA
	R	Pull-up Resistor			30		kΩ
21–22–23–24 X4, X3, X2, X1 } Keyboard Out	V_{OL}		V_{DD} = 4.75 V, I_{OL} = 1 mA			0.4	V
	$I_{O\ (off)}$		$V_{O\ (off)}$ = 5.5 V			25	µA
25–Mains On Enable	V_{IL}					0.8	V
	V_{IH}			2.4			V
	I_{IL}		V_{DD} = 5.25 V			–0.4	mA
	R	Pull-up Resistor	V_{IL} = 0.8 V		30		kΩ
26–Mains On/Off	V_{OL}		V_{DD} = 4.75 V, I_{OL} = 100 µA			0.4	V
	I_O		V_{DD} = 4.75 V, V_O = 0.7 V	–1.6			mA
31–Z2 32–Z1 MPX for Display Out	V_{OL}		V_{DD} = 4.75 V, I_{OL} = 1 mA			0.4	V
	$I_{O\ (off)}$		V_{DD} = 5.25 V, $V_{O\ (off)}$ = 13.2 V			50	µA
37–UHF 38–CATV 39–VHFIII 40–VHFI } BAND	V_{OL}		V_{DD} = 4.75 V, I_{OL} = 1 mA			3	V
	V_{OH}		V_{DD} = 4.75 V, I_{OH} = – 150 µA	2.4			V
	V_{IL}					0.3	V
	V_{IH}			3			V
	$I_{O\ (off)}$		V_{DD} = 5.25 V, $V_{O\ (off)}$ = 13.2 V			50	µA
27-28-29-30-33-34-35 Display Out	V_{OL}		V_{DD} = 4.75 V, I_{OL} = 20 mA			1.5	V
36-Display Out	V_{OL}		V_{DD} = 4.75 V, I_{OL} = 30 mA			1.5	V
31-Memory 8/16	V_{IH}			2.0			V
	V_{IL}					0.8	V

491B-03.TBL

DESCRIPTION (All timings at f_{clock} = 500kHz)

PIN 1 : V_{SS}

The substrate of the IC is connected to this pin. This is the reference pin for all parameters of the IC.

PIN 2 : MEMORY SUPPLY VOLTAGE

A supply voltage of 25 ± 1 V has to be applied to this pin during the modify and read cycles.

MODIFY CYCLE

A modify cycle consists of three steps :

1. All ”1”s are written in the bits of the selected word.
2. All bits of the selected word are erased (all ”0”s)
3. The new content is written.

Thus a constant aging of all the bits of the word is obtained.

During both write and erase cycles the memory status is checked continuously ; therefore after each write or erase pulse a read operation is carried out. The write or the erase operations are stopped as soon as the result of the read operation is valid.

WRITE CYCLE. The peak of the current flowing through pin 2 during a write operation is shown in fig. 1, while fig. 2 shows the envelope of the same current.

The typical write time is 3-4 ms for the first cycles and increases to about 30 ms after 1000 cycles.

Figure 1

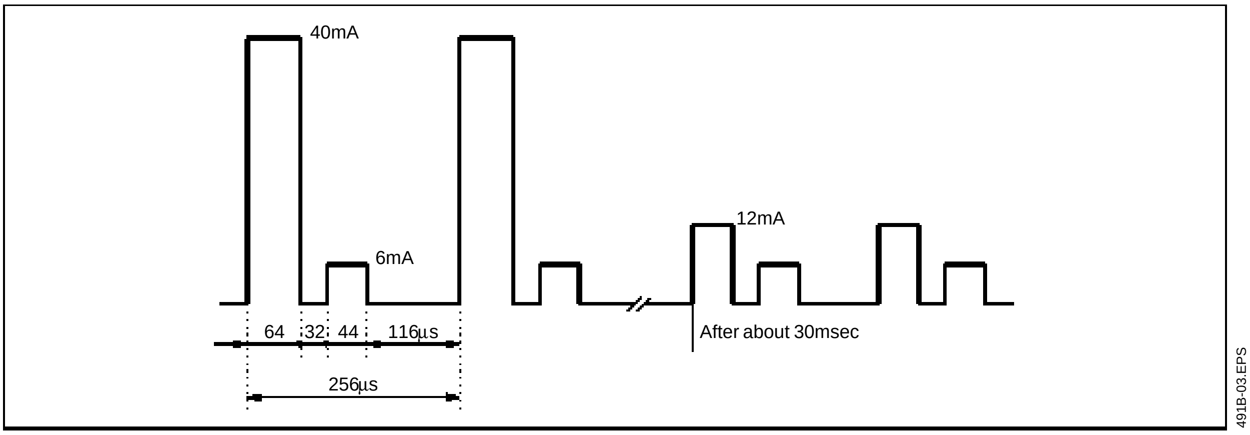
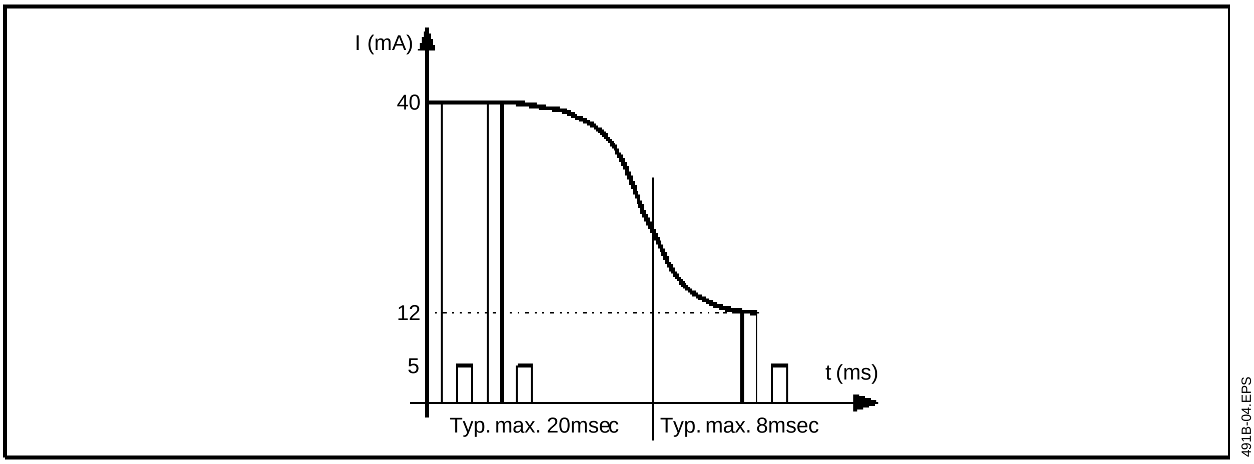


Figure 2



ERASE CYCLE

Figure 3 shows the timing and the waveform of the current flowing through Pin 2 during the erase operation. The peak current is 7mA (max) during the erase cycle and 6mA (max) during the read cycle. The typical erase time is 10ms for a new device and increases with the number of modify operations up to 200ms after 1000 cycles.

In order to protect the memory in case of failure of some bits the modify operation is stopped after 1sec.

READ CYCLE

Figure 4 shows the waveform of the current during a read operation.

Figure 3

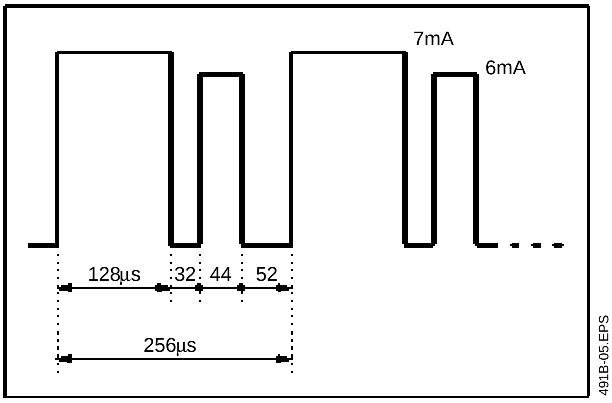
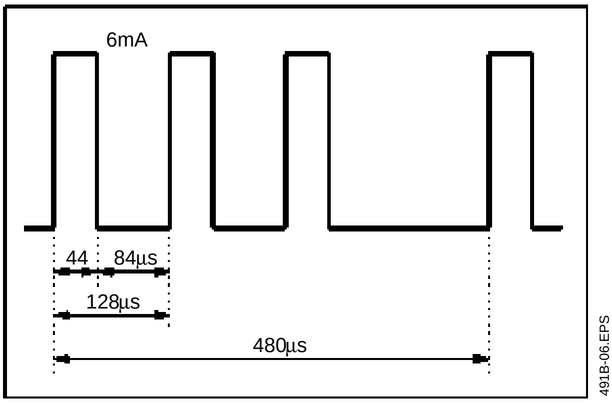


Figure 4



PIN 3 : MEMORY TIMING OUTPUT
This output gives the timing for the pulses to be applied at Pin 2 during the modify and read cycles. The output consists of an open drain transistor.

PIN 4 : FINE TUNING D/A (see Figure 5)
A D/A converter with 16-step resolution and a frequency of 15kHz can be used to generate a voltage which, if fed to a varicap diode in parallel to the AFC discriminator, will detune the receiver by a small Δf while maintaining the action of the Digital AFT. This output can be used in conjunction with both Linear and Digital AFT modes of operations.

The Fine tuning function operates as follows :
- At the start of any automatic or manual search, the output is set at the mid range.
- When the search has been completed it is possible to operate on FT ± commands.
  The store command memorizes this information together with the 13 tuning voltage bits and 2 information bits.
- Modification time of FT D/A is of 1 step every 200ms if issued locally or every 2 received signals from Remote control transmitter.

PIN 5 : TUNING D/A (see Figure 6)
A 2^{13} = 8192 step pulse modulated signal for the tuning voltage is available on this pin.

Pulse modulation is implemented by combination of a rate multiplier and pulse width principle.

With a tuning voltage increasing from zero, the number of pulses increases continuously up to 2^8 = 256 ; starting from this point the number of pulses remains the same but the pulses get larger until they reach the maximum content of the internal counter. The output consists of an open drain transistor which offers a low impedance to ground when in the ON state.

Figure 5

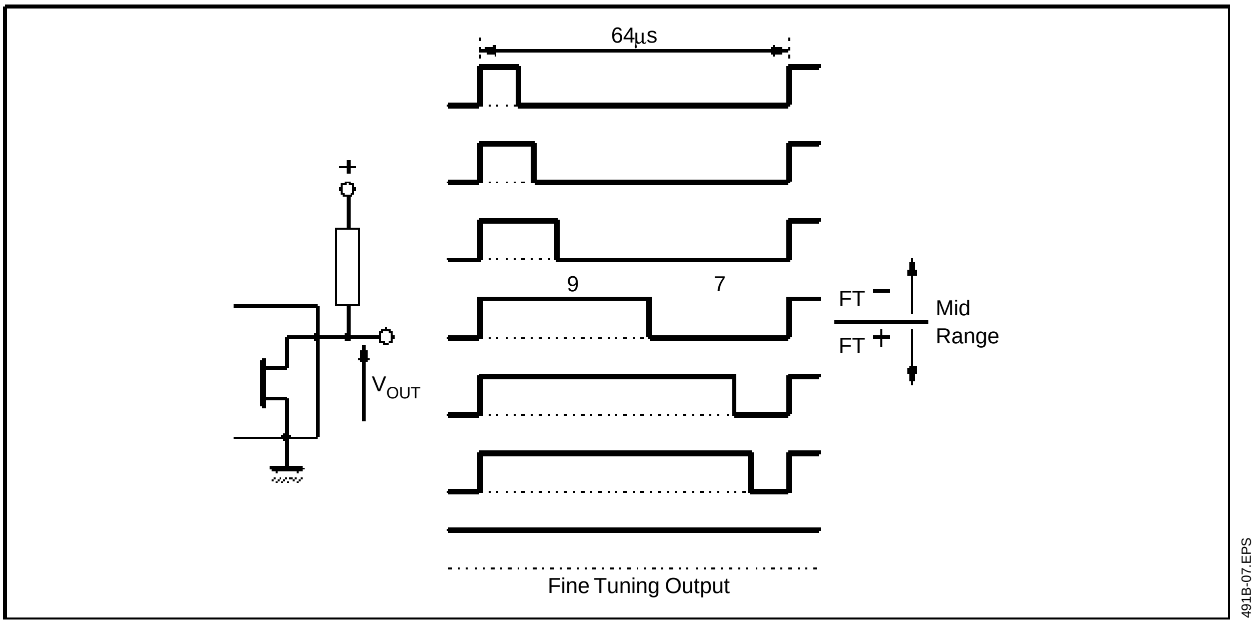
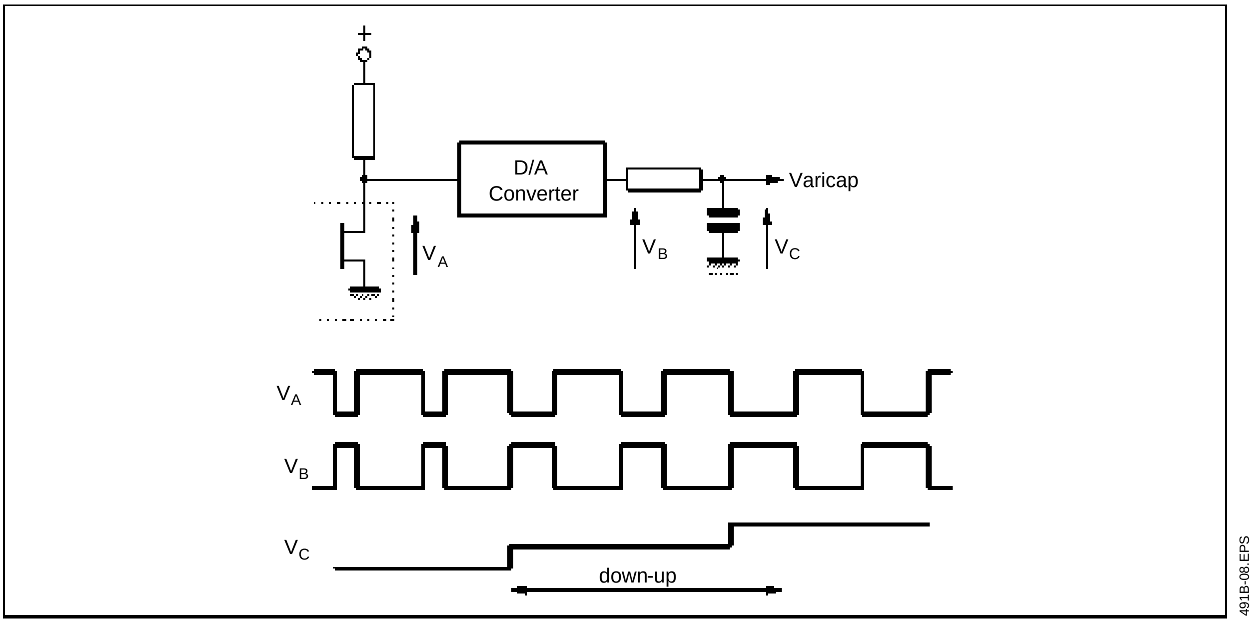


Figure 6



PIN 6 : DIGITAL AFT STATUS OUTPUT (see Figure 7)

This output shows the status of the digital AFT. It is low when the digital AFT is enabled and it can directly drive a LED.

The output consists of an open drain transistor.

PINS 7 & 8 : OSCILLATOR INPUT/OUTPUT (see Figure 8)

The frequency of the clock oscillator should be between 445 and 510kHz using a low-cost ceramic resonator. In these conditions the value of the reference frequency of the transmitter can be in the same range. In other words the transmitter and the receiver can operate with different reference frequencies.

Figure 7

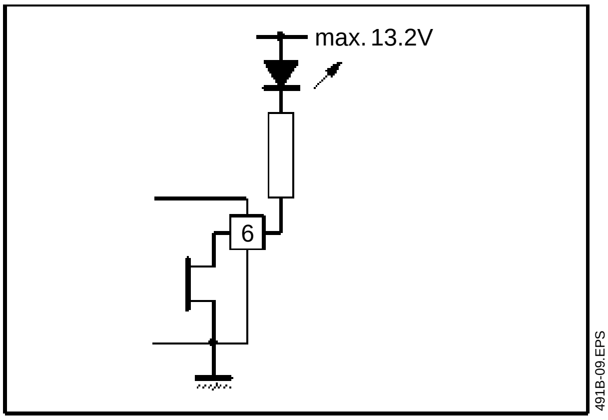
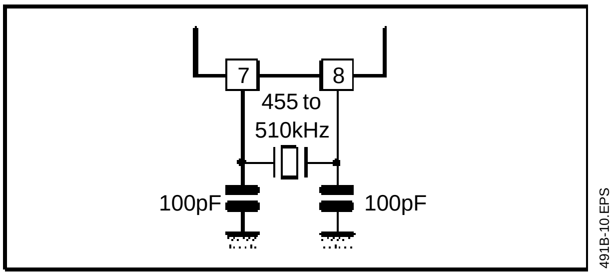


Figure 8



PIN 9 : V_{DD}

The supply voltage has to be comprised in the range 4.75 to 5.25V. When it is applied an internal power on reset of 0.5s is generated.
The memory position 1 is automatically read if the mains on option input (Pin 25) is grounded.

PIN 10 : TEST

This pin is used for testing and has to be connected to V_{SS}.

PIN 11 : I.R. SIGNAL INPUT (see Figure 9)

The integrated receiver decodes signals transmitted by M708, address 9.
The minimum signal to be applied is 0.5V peak-to-peak. (AC-coupled).
The receiver input section performs the following tests on the incoming signal to achieve the necessary noise immunity :

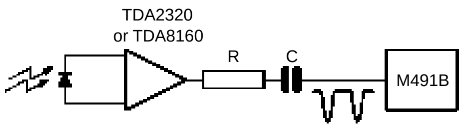
- measurement of the pulse distance (time base synchronization)

- check of the position of the received bits opening window at the time bases
- check of the parity bit
- check of the absence of pulses between the parity bit and the stop pulse
- check of noise level ; the receiver checks parasitic transients inside and outside the time windows.

If the above test conditions are not fulfilled, the received word is rejected and not decoded. If the received signal is acknowledged as a valid word it is stored an decoded.

The end of transmission will be acknowledged by receiving the end of transmission code or by means of an internal timer if the transmission remains interrupted for more than about 550ms.

Figure 9



Supply Voltage of TDA2320	R	C
5	2.2kΩ	4.7nF
12	10kΩ	4.7nF

491B-11.EPS

M491B REMOTE CONTROL RECEIVER TRUTH TABLE. Transmitter M708 ; Address Code 9

Command Number	I.R. Code						Function
	C1	C2	C3	C4	C5	C6	
0	0	0	0	0	0	0	End to Transmission
1	1	0	0	0	0	0	Power On/Off
2	1	1	0	0	0	0	Mute On/Off
3	0	0	1	0	0	0	Memory 1
4	1	0	1	0	0	0	Memory 2
5	0	1	1	0	0	0	Memory 3
6	1	1	1	0	0	0	Memory 4
7	1	0	0	0	1	0	Fine Detuning Up
8	1	1	0	0	1	0	Fine Detuning Down
9	0	0	1	0	1	0	Memory 5
10	1	0	1	0	1	0	Memory 6
11	0	1	1	0	1	0	Memory 7
12	1	1	1	0	1	0	Memory 8
13	1	0	0	0	0	1	Memory Up
14	1	1	0	0	0	1	Memory Down
15	0	0	1	0	0	1	Memory 9
16	1	0	1	0	0	1	Memory 10
17	0	1	1	0	0	1	Memory 11
18	1	1	1	0	0	1	Memory 12
19	1	0	0	0	1	1	Manual Search Up
20	1	1	0	0	1	1	Manual Search Down
21	0	0	1	0	1	1	Memory 13
22	1	0	1	0	1	1	Memory 14
23	0	1	1	0	1	1	Memory 15
24	1	1	1	0	1	1	Memory 16
25	1	0	0	1	1	1	Volume Up } Mute
26	1	1	0	1	1	1	Volume Down } Mute
27	0	0	1	1	1	1	Memory Addressing
28	1	0	1	1	1	1	Digital AFT On
29	0	1	1	1	1	1	Band Sequential
30	1	1	1	1	1	1	Automatic Search

491B-04.TBL

PINS 12 & 13 : AFT1-AFT2 (STOP/AFT INPUTS)

These pins are enabled during the automatic search and during normal operation, when the digital AFT is enabled (see description of Pin 17).

The STOP/AFT inputs are also disabled internally during any program or band change for the duration of the Mute signal.

These pins work according to the truth table given below :

M491B Pin 12 TDA4433 Pin 2	M491 B Pin 13 TDA4433 Pin 6	Function (referred to the tuning voltage)
H	L	Up
L	H	Down
L	L	Middle
H	H	No Operation

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These inputs have two different functions depending on whether the system is in the search or in normal operation (AFT control).

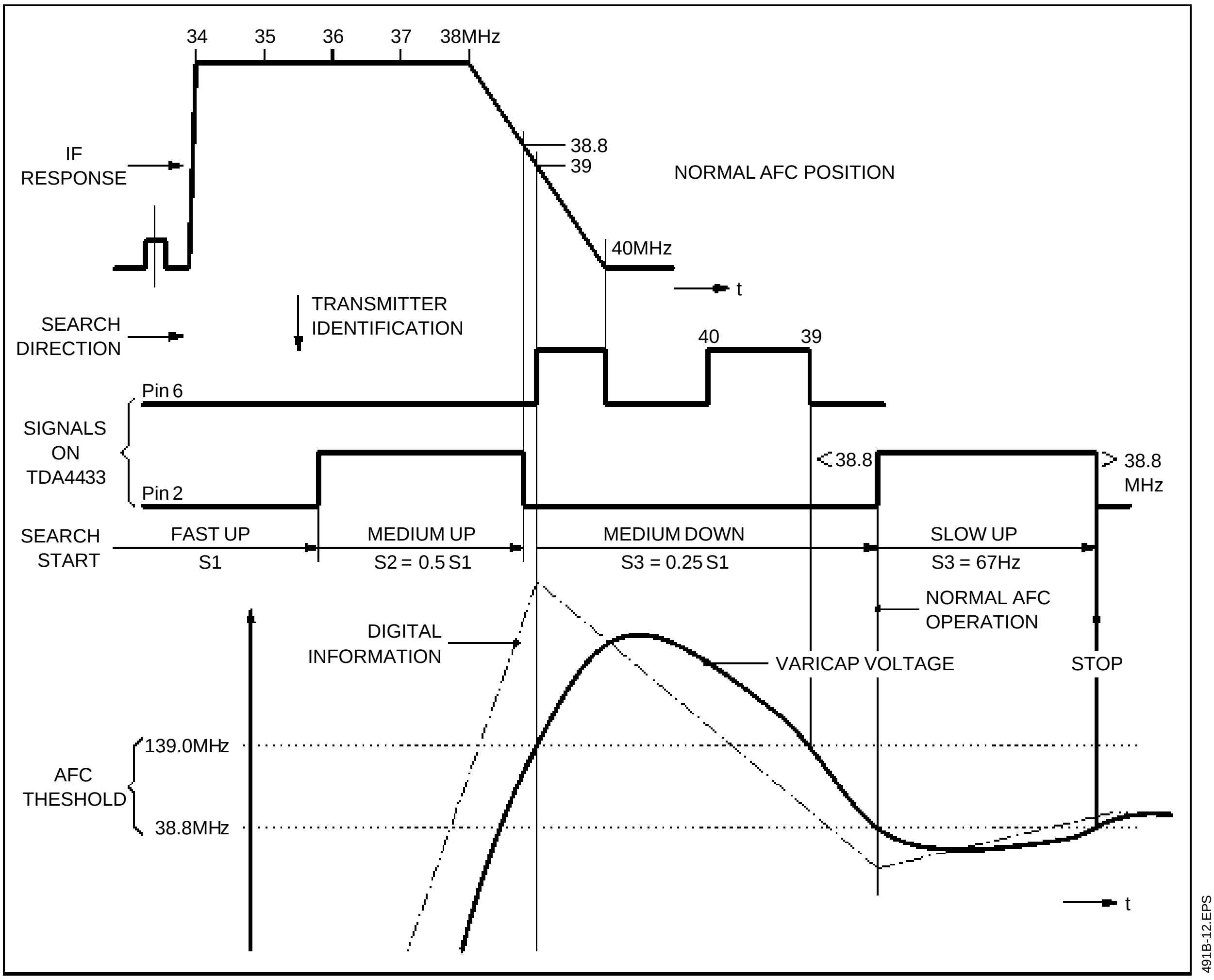
The inputs have internal pull-up resistors of 30kΩ typ.

A) **Search mode :** after depressing the Automatic search or preset keys, the levels of the signals coming from the TDA4433, applied to these pins, control the search function and determine when the search must stop, i.e. a TV station has been recognized.
The circuit operates in the following sequence (see Figure 10 for reference) :
1 - after pressing the search start key the search occurs in the FAST UP mode.
2 - eventual transitions available on these inputs are ignored during the first 15 search steps if the system is in the UHF or CATV bands.
If the system operates in VHF I and III bands, the first 60 search steps are ignored. The acceptance delay of 15 (60) search steps has been introduced to prevent the system from stopping at the previous station.
After this time the FAST UP speed is automatically reduced to half during each UP signal (MEDIUM UP = FAST UP/2).
A DOWN signal preceded by at least an UP signal will set the search to MEDIUM DOWN mode (FAST UP/4).
3 - the next UP signal will switch the search to SLOW UP speed (61Hz).
At this point the systems is in normal AFT operation.

B) Digital AFT operation : when a station is perfectly tuned, the input signals coming from TDA4433 are at middle condition.
If the tuning moves lower than the threshold below 38.9MHz, the Pin 12 is put H and Pin 13 is put L ; the 13 bit internal counter is moved SLOW UP speed to increase the varicap voltage.
When a detuning occurs in the opposite direction the input 12 goes Low and 13 goes High and the tuning voltage falls at VERY SLOW DOWN speed (7.6Hz).
The increase or decrease of the tuning voltage is stopped as soon as the input returns to middle conditions.
Therefore during normal operation Pins 12 and 13 act as digital AFT control commands.

C) **Recall from memory :** when the digital AFT is enabled and data is recalled from Memory, a fixed value of 8 steps (≈ 31.2mV) is subtracted from the tuning voltage.
This corresponds to a detuning of 0.6MHz (UHF) and of 0.3MHz in VHF III into that part of the IF response curve which corresponds to the fully transmitted sideband.
At this point the AFT operation takes over as described in point B above and the exact tuning is achieved in about 0.2 sec.
This feature increases the AFT capture range and fullfills the stability requirements of the tuner, voltage references and the D/A converter.
If the Digital AFT is disabled (Pin 17 at V_{SS}), the memory content is read without any change.

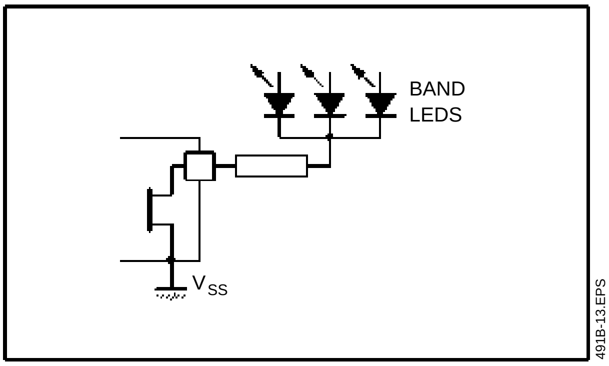
Figure 10



PIN 14 : SWEEP SEARCH DISPLAY OUTPUT

This output, which is normally Low, goes High during automatic search automatic preset et intervals of 160ms for about 40ms to blank the LED of band display.

Figure 11



PIN 15 : VOLUME D/A OUTPUT

This output delivers a square wave signal of 7.8 kHz and duty cycle variable in 63 steps. In case of a continuous command for varying the volume, the duty cycle is changed at the rate of the transmitted signal (approximately every 102ms with f_{ref} = 500kHz) or every 112ms if issued locally.

Overflow and underflow protection are provided.

The volume output can be switched to V_{SS} and reset to the previous level by means of the Mute On/Off command. It is also reset by the Volume Up/Down and the Mains On/Off commands.

The volume is muted for about 1s at each mains on and off command during the power on reset time and program change (0.5s).

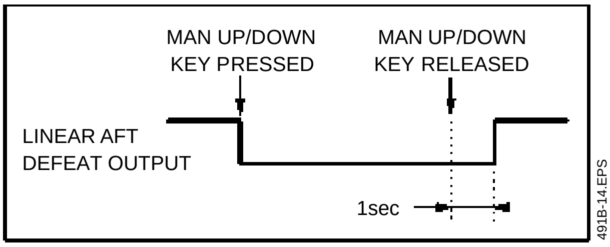
At the first power on reset of V_{DD} the volume D/A is set at the level 21/64. The last level is preserved until V_{DD} is not removed.

PIN 16 : LINEAR AFT DEFEAT OUTPUT

This output is normally High and goes Low when a Manual Up/Down command is issued.

It returns High with a 1 second delay from the release of the key, in order to give the user the possibility of the tuning adjustment without the AFT intervention. It goes Low for 0.5s during program change.

Figure 12



PIN 17 : DIGITAL AFT ENABLE INPUT

If this input is connected to V_{SS} (GND), the digital AFT loop is always disabled. If pin 17 is left open or is connected to V_{DD}, the digital AFT is automatically enabled at power on. When a manual up/down search command is issued, the digital AFT loop is disabled and the digital AFT status output is inhibited.

The digital AFT loop is restored by the commands: Digital AFT on/Automatic search/Automatic preset.

PINS 18-19-20-21-22-23-24 :
KEYBOARD MATRIX (see Figure 13)

A command is accepted if the corresponding contact has been closed for a minimum time of 30ms.

Local input commands and I.R. commands have the same priority.

If a complete I.R. command has been received, the local inputs are blocked until the command has been executed and the "end of transmission code" generated.

Viceversa an I.R. signal cannot be decoded until an issued local command has been executed.

MEMORY UP/DOWN

Depressing one of these two commands, the memory position is stepped in the UP or DOWN direction.

If the key is kept closed, the channels are stepped UP/DOWN every 0.5 second or every 5 commands from the transmitter.

The memory locations 9 to 16 are jumped if pin 31 is at GND level.

BAND SELECTION

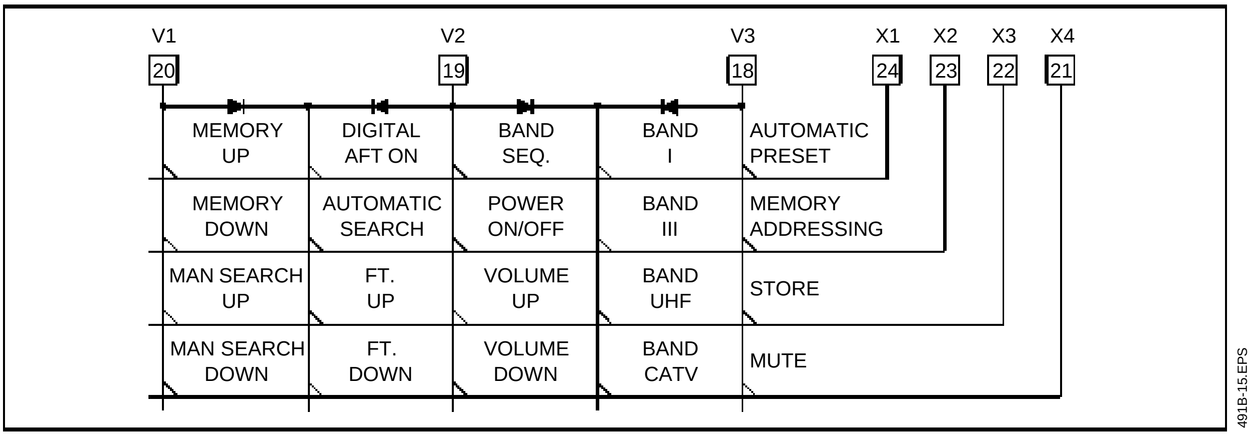
The bands can be selected either directly or with a step-by-step command in the following sequence :

VHF I
CATV
VHF III
UHF
VHF I and so on

Only one band change is performed at each accepted command.

Disabled bands are automatically skipped. A band can be disabled connecting the corresponding output to V_{SS}.

Figure 13



SEARCH MODES

4 modes are available :

a) Automatic search ⎤ (digiatl AFT)
b) Automatic preset ⎦
c) Manual up/down (digital and linear AFT)
d) Manual up/down (linear AFT)

a) AUTOMATIC SEARCH. The search starts from the actual tuning and band position. During the search the tuning voltage is always changing from lower to higher voltage levels. When the end of the band is reached the search restarts from the beginning of the next band after a 480 ms interruption with the sequence of step-by-step band selection. Disabled bands are automatically skipped.

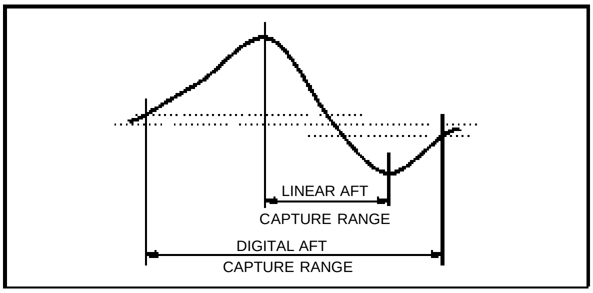
The search is stopped when the first station is found or if a channel selection command is given.

Stop of the automatic search is determined by the STOP/AFT inputs controlled by the TDA4433 which converts the AFC-S-curve into an up/down command.

At the end of the search the up/down command controls the correct tuning acting on the counter of the voltage synthesizer (Digital AFT).

It is important to call the attention to the Digital AFT capture range which is larger than the normal linear AFT as shown in fig. 14.

Figure 14



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Additionally the use of the Digital AFT allows storage of the tuning information corresponding to the zero point of the AFC-S-curve. This cannot be guaranteed using the Linear AFT method only. The latter is a cheaper system, because it does not require the use of the TDA4433 but it cannot guarantee what described above.

As a result of the use of the Digital AFT, the requirements for stability of the tuner, of the reference voltage source and of stability of the D/A converter are less critical.

Tuning speed in automatic search, if no station is found is :

VHF I	8 second
VHF III	8 second
UHF	32 second
CATV	32 second

The tuning and band information can be stored using the store/memory addressing command.
The search can be stopped by a memory selection command.

b) AUTOMATIC PRESET. The search starts from the lowest memory address, tuning voltage and VHF I band as described in automatic search mode.

When an active station is encountered, the corresponding tuning and band information is automatically stored in the Non-Volatile Memory.

Afterwards the system starts to search for the next station. The cycle is repeated until all bands have been scanned or the tuning information has been stored into all address locations. After completing this cycle the system reads out the tuning information of the lowest address.

c) MANUAL UP/DOWN WITH DIGITAL AND LINEAR AFT (pin 17 at V_{DD}). Holding one of these commands pressed, the tuning voltage is increased or decreased.

During this operation, the Digital AFT is automatically defeated and can only be reconnected with the "AFT on" command or by an Automatic search or preset command.

The search speed is kept at minimum (there is no increment with the time)

Band	Sweep Timefor the Complete Band	Number of Tuning Steps/Second
VHF I	128 seconds	64
VHF III	128 seconds	64
UHF	512 seconds	16
CATV	512	
seconds	16	

In case of command received from remote control, the counter is increased/decreased every two received commands.
No band switching is provided at the upper or lower tuning positions.
The volume is automatically muted 3 second after the key pressure is immediately restored at the release of the key.

d) MANUAL UP/DOWN WITH LINEAR AFT (pin 17 at V_{SS}). When this control is used the Digital AFT is disabled.

The Linear AFT output goes low after an up or down command is issued and remains Low for 1 second after the release of the key.

The volume is automatically muted for 3 seconds after the key pressure and is immediately restored at the release of the key.

Tuning speeds are as follows :
- FINE TUNING UP/DOWN
  See description of pin 4.
- DIGITAL AFT ON
  See description of pin 17.
- VOLUME UP/DOWN
  See description of pin 15.
- MAINS ON/OFF
  See description of pins 25 and 26.

Band	Number of Tuning Steps Second			
	Time 0	After 1 s	After 2 s	After 3 s
VHF I	64	128	256	512
VHF III	64	128	256	512
UHF	16	32	64	128
CATV	16	32	64	128

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STORE COMMANDS

2 modes of operations are available.

a)store
b)memory addressing

In order to protect the memory, the store function is internally disabled after one store cycle.
It is enabled after a program change or a tuning operation (it is not disabled by the Digital AFT control).

a) STORE. The tuning information (Tuning D/A, Fine tuning D/A and band) is stored in a previously selected memory address when this command is issued.

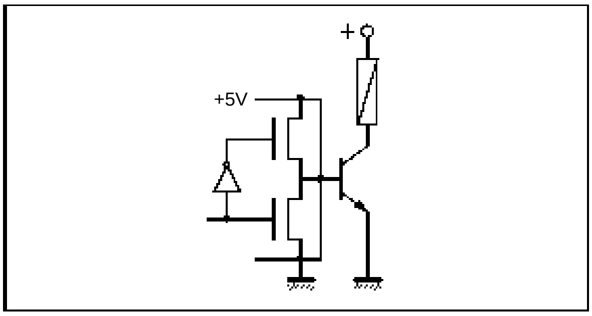
b) MEMORY ADDRESSING. The tuning information can also be stored with this command followed by the memory position selection.
When this command is accepted all the memory LEDs are blanked.
Selection of the memory position initiates the store operations and restores the display.

MUTE ON/OFF
See description of pin 15.

PIN 25 : MAINS ON OPTION INPUT
If connected to V_{SS} (GND) the Mains output is automatically switched on when V_{DD} is applied and memory 1 is read.
If it is connected to V_{DD} the circuit goes in stand by condition.

PIN 26 : MAINS ON/OFF OUTPUT
Switch on of the set is controlled by the Mains on command issued for more than 0.3 s. The output transistor is set in the off condition to drive through an integrated pull-up resistor, an external NPN transistor.

Figure 15



491B-17.EPS

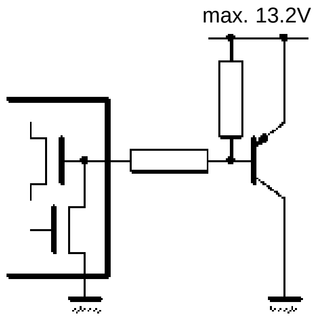
At each Mains on command a memory read out occurs. A V_{PP} (+ 25 V) is required for this operation, a 1 second delay starts when the mains output is switched off. For a correct reading of the memory the V_{PP} supply voltage must reach the value of 25 V within 1 second after a Mains on command.
In case of automatic switch on at power on caused by pin 25 at GND, the total delay is of 1.13 second (0.13s for V_{DD} power on reset plus 1 second for mains on).
The Mains on/off command, if repeated, will switch the output on (set off).
The last address information is preserved until V_{DD} is present.
Next Mains on command will switch the set at the previously selected memory address and a read operation will be performed.

PINS 27-28-29-30-33-34-35-36 :
MEMORY ADDRESS OUTPUT
These pins operate as output only for display of the selected memory location. Max drive capability is of 15 mA/1.2 V with the exception of pin 36 that is of 30 mA/1.5 V.
Direct memory selection is only possible by remote control. A local memory up/down command is available in case of emergency.
Pin 32 must be grounded.
If pin 31 is grounded, the memory position 9 to 16 are skipped in case of memory up/down commands.
For normal operation pin 31 can be left open or, better, connected to V_{DD}.

PINS 31-32
See description of pins 27 to 30 and 33 to 36.

PINS 37-38-39-40 : BAND INPUT/OUTPUT
These outputs are provided to select up to 4 bands via external PNPs.
If one or more bands have to be skipped, the corresponding outputs have to be short-circuited to V_{SS}.

Figure 16

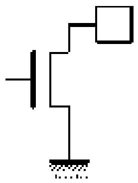


The relation between pins and bands are as follows :
Pin 37 = UHF
Pin 38 = CATV
Pin 39 = VHF III
Pin 40 = VHF I

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INPUT/OUTPUT CONFIGURATION

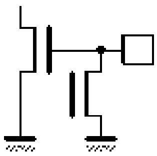
Output Open Drain



Pins 3, 4, 5, 6, 14, 15, 16, 30, 33, 34, 35, 36

491B-19.EPS

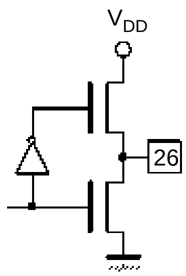
Inputs/Outputs (std)



Pins 37, 38, 39, 40, 21, 22, 23, 24
(21, 22, 23, 24 are used only for testing purposes)

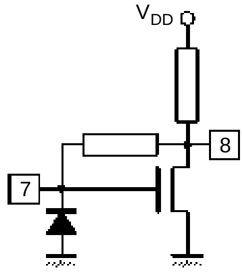
491B-22.EPS

Output Push-pull



491B-20.EPS

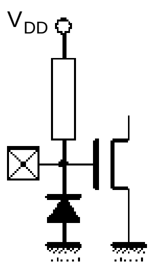
Oscillator



491B-23.EPS

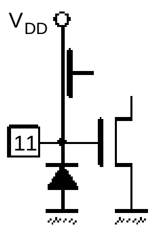
Inputs with Pull-up Load

Pins 12, 13, 17
18, 19, 20, 25, 31



491B-21.EPS

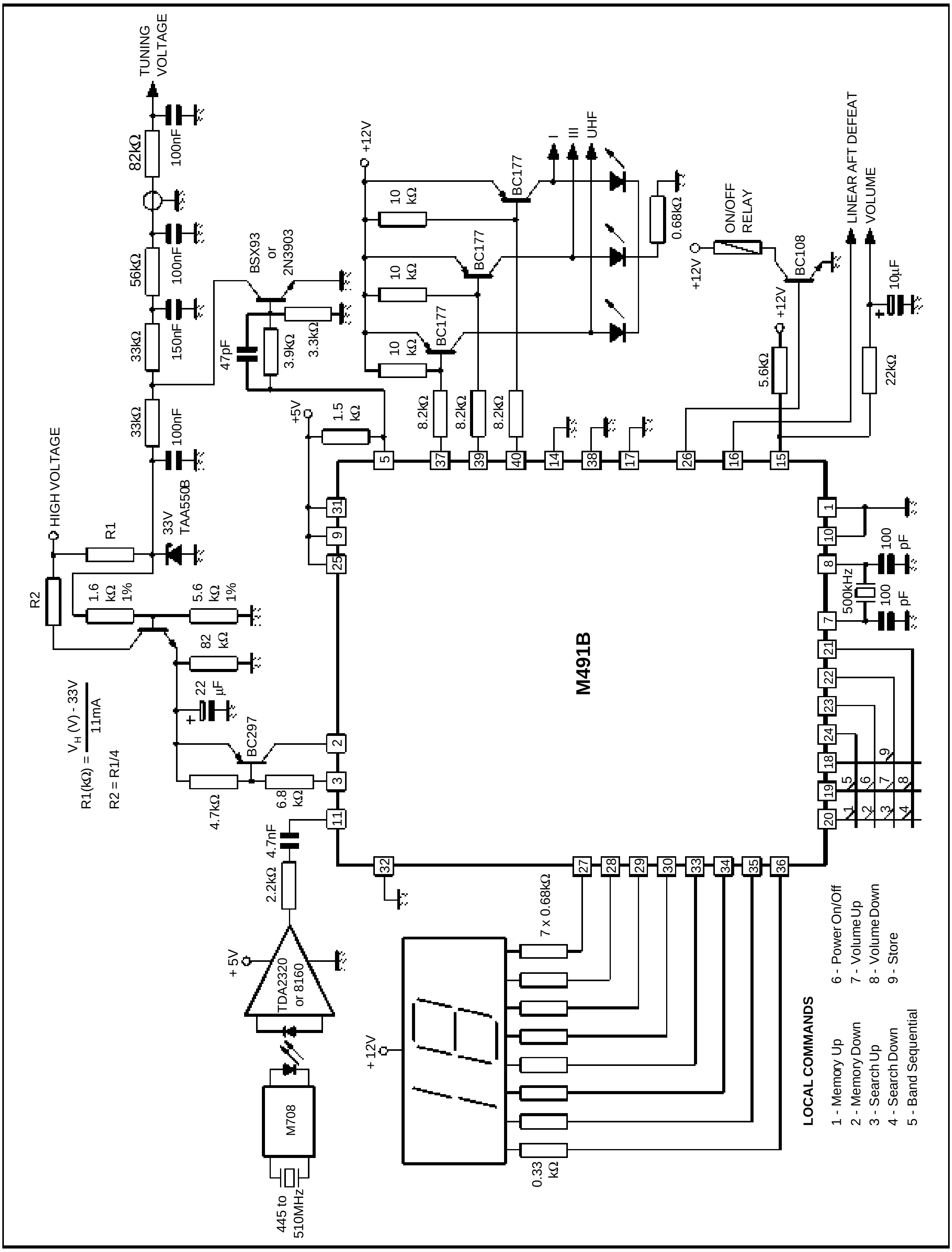
IR Input



491B-24.EPS

TYPICAL APPLICATION

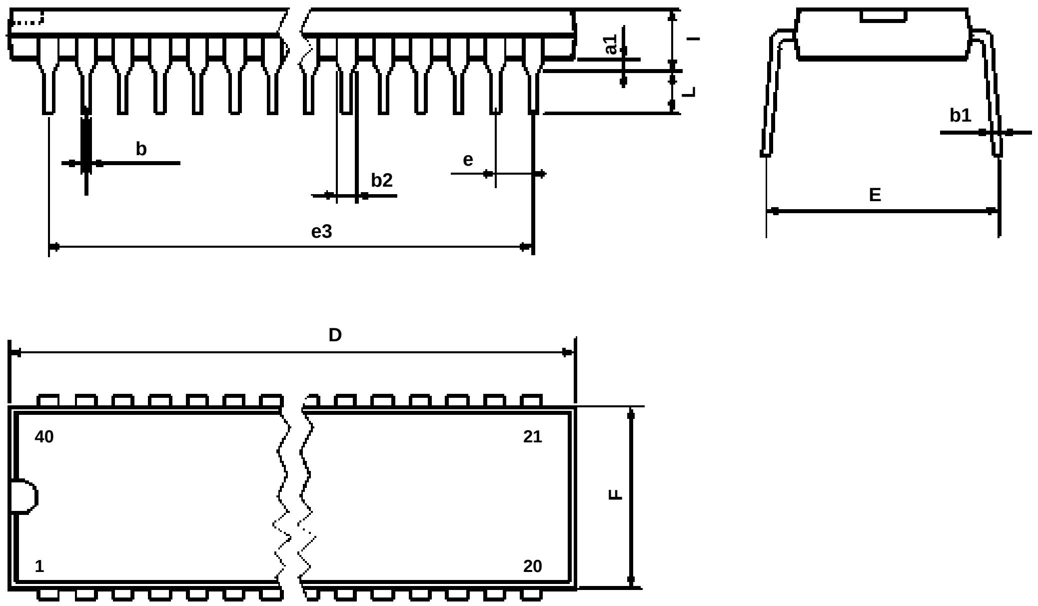
Manual Search with Linear AFT (16 memory option)



491B-25.EPS

PACKAGE MECHANICAL DATA

40 PINS - PLASTIC DIP



PM-DIP40.EPS

Dimensions	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
a1		0.63			0.025	
b		0.45			0.018	
b1	0.23		0.31	0.009		0.012
b2		1.27			0.050	
D			52.58			2.070
E	15.2		16.68	0.598		0.657
e		2.54			0.100	
e3		48.26			1.900	
F			14.1			0.555
i		4.445			0.175	
L		3.3			0.130	

DIP40.TBL